

Criteria	Ratings	Expectation
<b>Summary/Abstract</b>	<b>10.0 pts</b>	
The summary/abstract should effectively explain the goals of the lab, the procedure, and results briefly but thoroughly.	The goals, procedure and results are summarized briefly but thoroughly.	In one or two sentences answer each of the questions: (1) What are the goals of the lab? (2) What is the procedure to accomplish the goals of the lab? (3) What are the results for the lab (what does the final design do?)
<b>Introduction</b>	<b>10.0 pts</b>	
Discuss relevant background material for the experiment, and what the objectives are. What concepts and theories are we testing? What applications do these concepts have for engineering? Why do we need to learn these things (objectives)? What is the background material behind the theories? Was any other relevant theory used?	Objectives, concepts, theories are clear. Possible applications of concepts clear. Relevance of learning objectives is well described.	Teach the reader the information needed to complete the lab. What is the objective (repeated from the Summary section), and give the information that is used to complete these objectives? Give at least one example of possible application.
<b>Procedure</b>	<b>15.0 pts</b>	
What steps were taken in the laboratory to carry out the experiment? Try and be detailed, show me that you understand what is going on. Use equations, figures, and schematics where you feel pertinent. You need to discuss the 'how' of carrying out these steps in more detail.	The steps taken to create the design are well documented. All equations, design specifications, truth tables, etc. are included and clear.	What are the design specifications? SHOW TRUTH TABLES HERE. How did you complete the truth tables? Using equations, and diagrams to make your report clearer (including block diagrams). How did you implement your design in Verilog? How do you know it worked correctly?
<b>Results - Design Code</b>	<b>15.0 pts</b>	
Required Verilog design code and testbenches defined in the lab instructions are included.	Verilog design code is complete. Testbench files (if user created) are complete.	Take Screenshots, <i>not pictures taken with your phone</i> . Any code or testbench that you wrote must be shown in this section. And show/explain the "checkoff" if needed.
<b>Results - Simulation Results</b>	<b>15.0 pts</b>	
The relevant printed output from the simulation is included in this section.	Simulation results for all simulation steps are clear showing the design passed simulation.	Take screenshots of simulation results and show/explain the "checkoff" if needed.
<b>Results - Hardware Implementation</b>	<b>10.0 pts</b>	
Include photos of various conditions of your hardware implementation (different switch settings with LED views, etc.) even though you demonstrate your design to instructors.	Hardware implementation was demonstrated and checked off - or no hardware implementation required for this lab.	Take photos of your hardware implementation and show/explain the "checkoff" if needed.
<b>Conclusion</b>	<b>10.0 pts</b>	
The conclusion should summarize the entire lab report. Talk about any debugging. If you could not get the project to work, explain what you think the issue is, and provide evidence to support your hypothesis.	Good summarization. Good description of debugging.	Short and sweet -- summarize the entire lab report.
<b>Document Format</b>	<b>5.0 pts</b>	
Use template on Canvas - Cover Page - All tables and figures labeled - Correct file format (pdf) - Within the page limit. (typically 7-8 pages maximum, but subject to change)	Document follows format.	Use the correct naming format, use a cover page, label all your tables and figures, type your truth tables
<b>Attendance</b>	<b>10.0 pts</b>	
Check in on Canvas at the beginning of lab.	Finish check in	Lose these points if your attendance recording on Canvas is absent.

**NOTE:** Each lab report will be graded following this grading rubric, but the grading of lab screenshot will be only focusing on the results that are checked off by instructors in class (see detail in the Lab Screenshot Template on Canvas).