Lab 5a – Synchronous Logic – Introduction to Bit Storage Implementation

Introduction

As discussed in the videos you were introduced to several different bit storage designs:

- *Basic SR Latch*
- *Level Sensitive SR Latch*
- *Level Sensitive D Latch,* or *Transparent D Latch*
- *Edge Triggered D Flip Flop*

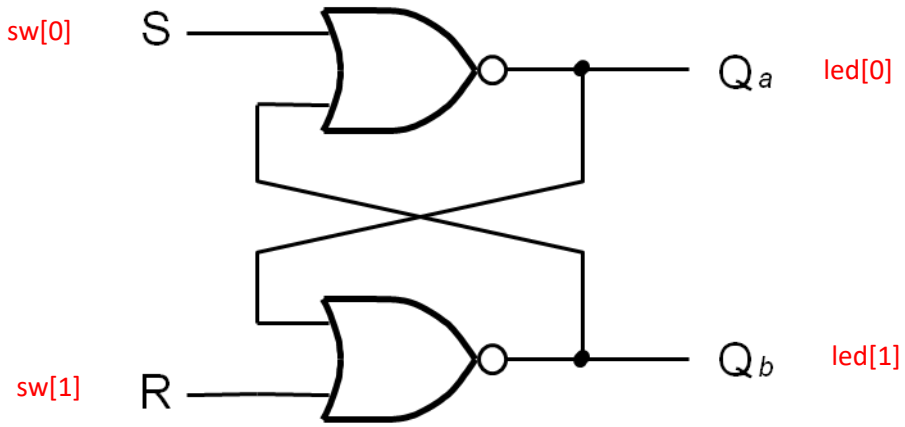
The latter device, the D flip flop, is the basic building block for all modern digital designs.

In this lab, you will go through the same design steps as was done in the videos, but now you will actually design each of these implementations of bit storage onto your hardware.

Detailed Specification:

Part A: Basic SR Latch

Here is the schematic for a Basic SR Latch from the videos, showing the final connections to your lab hardware design in red (switches, center push button and LED's):



You will have this module template to complete the design. You can use either gate primitive instantiations to make you NOR gates or assign statements.

```
module sr_latch (output logic qa, output logic qb, input logic s,
    input logic r);
…
endmodule
```

Part B: Level Sensitive SR Latch

Below is the schematic for a Level Sensitive SR Latch from the videos. Both the S and R inputs are now qualified by a clock signal, C.

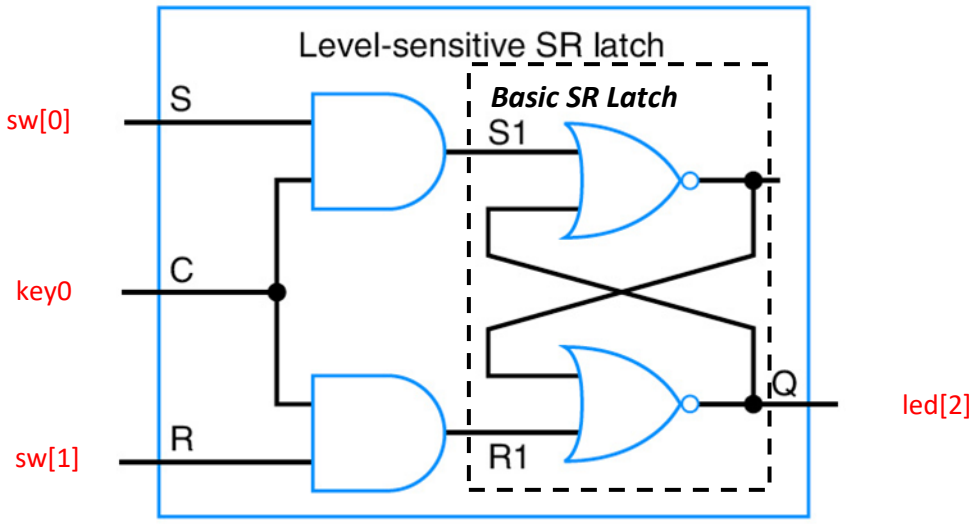


Figure 3.14 Level-sensitive SR latch—an SR latch with enable input C.

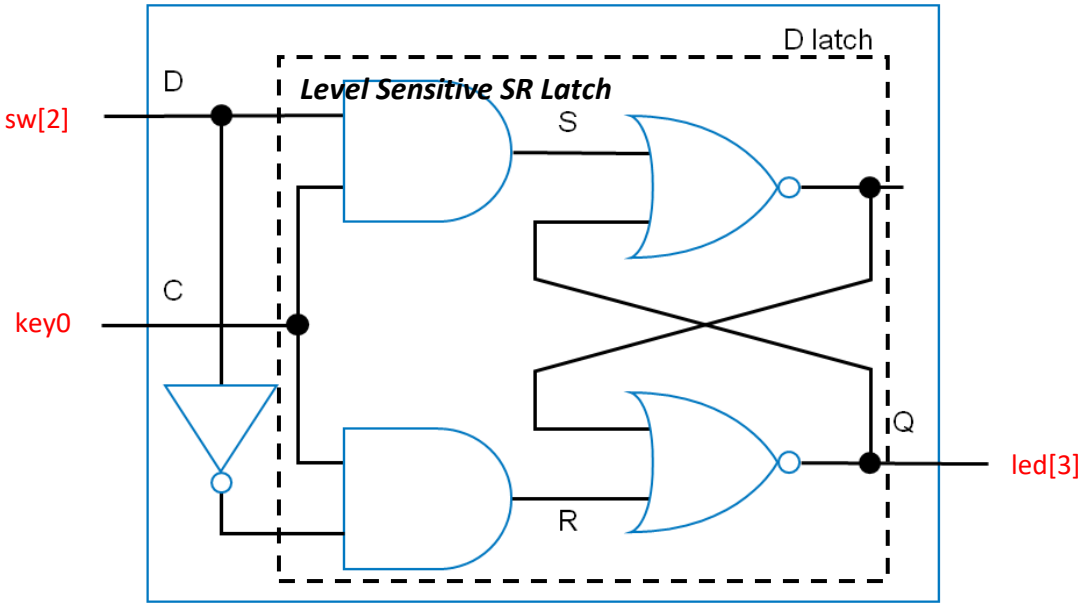
You will have this module template to complete the design. You should reuse (instantiate) the basic SR latch from part A and add the AND gates.

```
module lvl_sen_sr_latch (output logic q, input logic s, input logic r,
    input logic c);

    logic s1, r1;     // outputs of the AND gates
…
endmodule
```

Part C: Level Sensitive D Latch

Below is the schematic for a Level Sensitive D Latch from the videos. An inverter is added between the inputs to reduce the possible input conditions.



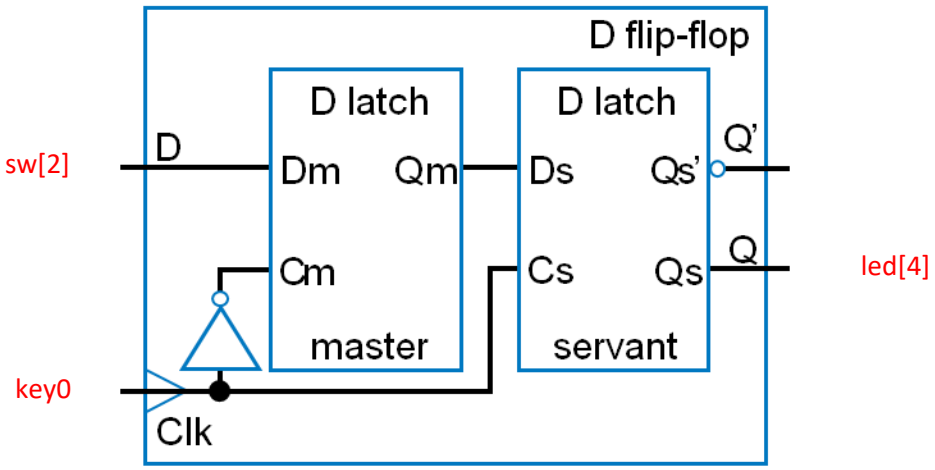
You will have this module template to complete the design. You should reuse (instantiate) the basic SR latch from part B and add an inverter. You can add the inverter several ways. The easiest is to use ~d (invert signal d).

```
module transparent_d_latch (output logic q, input logic d,
    input logic c);

…
endmodule
```

Part D: Edge Triggered D Flip Flop

Below is the schematic for an Edge Triggered D Flip Flop from the videos. Note two transparent D latches are used with the output of one feeding the input of the other, and the clock to each are inverted.



You will have this module template to complete the design. You should reuse (instantiate) the transparent D latch from part C and add an inverter. You can add the inverter several ways. The easiest is to use ***~d*** (invert signal ***d***). (You can skip the ***Q'*** output in the figure.)

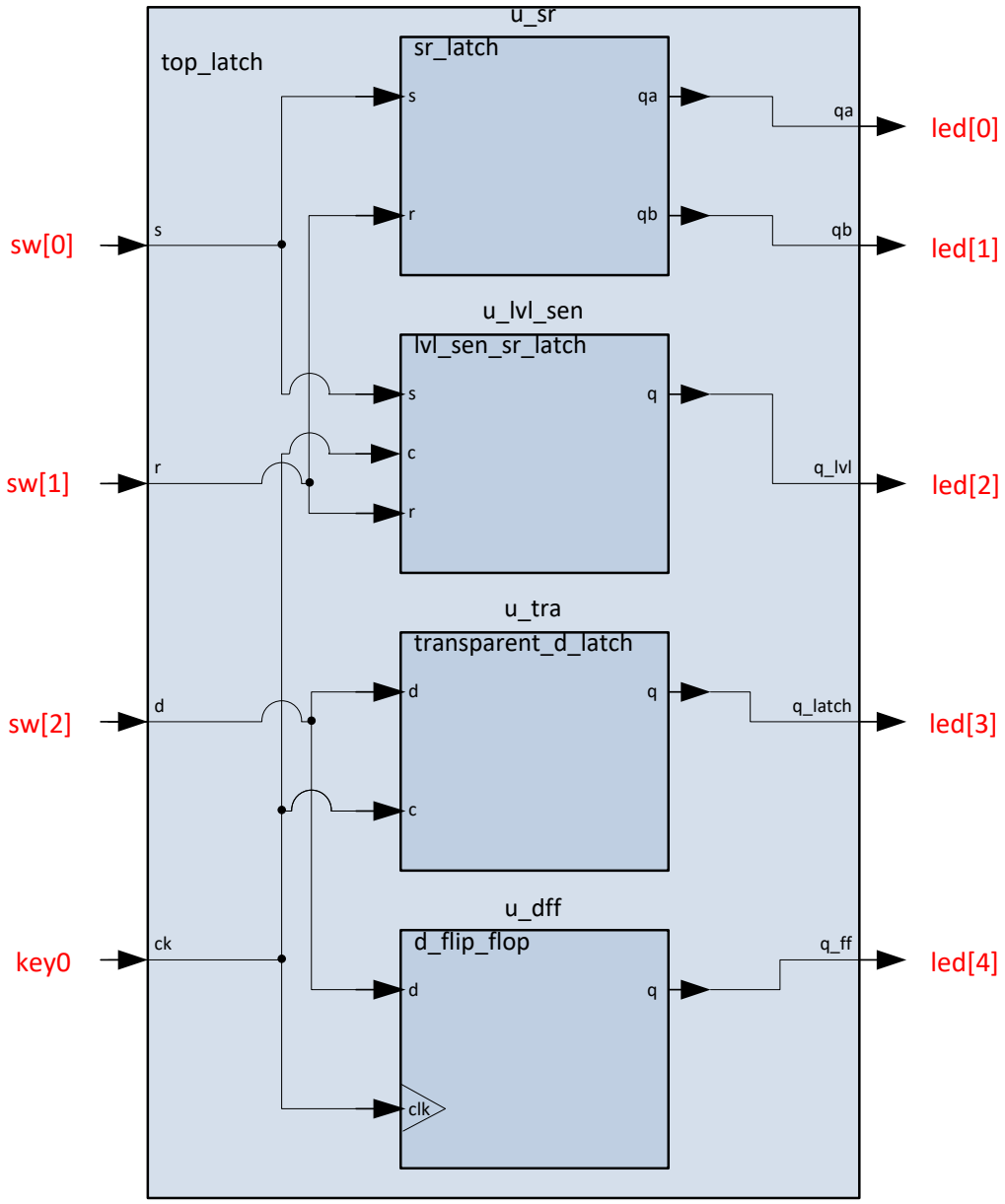
```
module d_flip_flop (output logic q, input logic d,
    input logic clk);

…
endmodule
```

Design/Modules

In this design you will need to complete the design of four modules described above.

You will then integrate them into one top module (***top_latch***) and which is connected to the hardware switches and LED's. A block diagram of this ***top_latch*** module is given below:



Summary of design steps - complete:

- Basic SR Latch (module ***sr_latch***)
- Level Sensitive SR Latch (module ***lvl_sen_sr_latch***)
- Level Sensitive D Latch (module ***transparent_d_latch***)
- Edge Triggered D Flip Flop (module ***d_flip_flop***)

- the wrapper that integrates them (module ***top_latch***)

Simulation/Verification

There is one testbench wrapper: ***tb_top_latch***

Running **top_latch.sim** will simulate the integrated design. This design shares many of the input signals as shown in the previous figures.

Below is an example of the timing diagram with the *D* and *CK* inputs, and *Q_latch* and *Q_ff* outputs. The second half of the diagram duplicates the input pattern of one of your workbook problems.

Synthesis

To synthesize your design, *right-click and run* on file: **lab5a_top.qsf**. It will take about a minute to synthesize, and the resulting output files will be in the **output_files** folder. The one you need to select and download is: **lab5a_top.sof**. Download this file to your local PC (*right-click and download*). Place this file in the shared folder you created.